AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. **(Currently Amended)** In a system that asserts a false synchronization signal at times when data is not present, a fiber-optic transponder that produces a lock signal only when data is present in a serial data signal, the transponder comprising:

~~an output adapted to couple to a host device;~~

a controller chip that includes a phase locked loop adapted to operate in a hunting mode and a locked mode, wherein the phase locked loop is further adapted to assert a synchronization signal in the hunting mode when a hunting frequency passes through a data signal frequency and wherein the phase locked loop is further adapted to keep the synchronization signal asserted as long as the phase locked loop is locked onto the serial [[a]]data signal; and

a timing circuit adapted to measure a period of time that the synchronization signal is asserted and to produce a lock signal if the synchronization signal is asserted for at least a specified period of time;

a demultiplexer arranged to receive a clock signal from the phase locked loop, the demultiplexer being configured to convert the serial data signal to a parallel data signal based on the clock signal.

2. **(Original)** The transponder of claim 1, wherein the timing circuit is an analog timer comprising a capacitor and a resistor network.

3. **(Original)** The transponder of claim 2, wherein the timing circuit comprises a transistor for resetting the timing circuit.

4. **(Currently Amended)** The transponder of claim 3, wherein the transistor is at least one of a field effect transistor, a PNP bipolar junction transistor, and NPN bipolar junction transistor.

5. **(Canceled)**

6. **(Previously Presented)** The transponder of claim 1, further comprising an input level detector that compares the synchronization signal with a reference signal and produces logical signals that are fed into the timing circuit.

7. **(Currently Amended)** The transponder of claim 2, the timing circuit further comprising a comparator that receives a signal from the capacitor and resistor network and a reference signal as input and that outputs the lock signal to a [[the]]host device based on the value of the reference signal compared to the signal from the capacitor and resistor network.

8. **(Original)** The transponder of claim 7, wherein the comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value.

9. **(Currently Amended)** A fiber-optic transponder comprising:

an output adapted to couple to a host device;

a controller chip having a phase locked loop that is adapted to operate in a hunting mode in which the phase locked loop briefly asserts a synchronization signal when a hunting frequency passes through a data signal frequency corresponding to a rate of data encoded in a data signal and that is adapted to operate in a locked mode in which the phase locked loop asserts the synchronization signal so long as the phase locked loop is locked onto the [[a]]data signal; and

a translation circuit adapted to convert the synchronization signal from the controller chip to a lock signal usable by the host device, wherein a logic level of the lock signal is asserted when the phase locked loop is locked onto a data signal and is de-asserted when the phase locked loop asserts the synchronization signal in hunting mode.

10. **(Previously Presented)** The fiber-optic transponder of claim 9, the translation circuit comprising a timer adapted to measure a period of time that the synchronization signal is asserted.

11. **(Previously Presented)** The fiber-optic transponder of claim 10, the translation circuit comprising an input level detector that acts as a comparator to the synchronization signal and a reference signal and that produces logical signals usable by the translation circuit to determine:

when the synchronization signal is asserted because the phase locked loop is locked onto a data signal, and

when the synchronization signal is asserted because a hunting frequency passes through a data signal frequency in hunting mode.

12. **(Original)** The fiber-optic transponder of claim 9, the translation circuit further comprising a comparator, wherein the comparator receives as an input a signal from the timer and a reference signal and outputs the lock signal for use by the host device based on a comparison of the signal from the timer and the reference signal.

13. **(Original)** The fiber-optic transponder of claim 12, wherein the comparator includes feedback that changes a logical level of the lock signal when the value of the lock signal changes by some value greater than a hysteresis threshold value.

14. **(Currently Amended)** A method of mediating signals from a controller chip used in a fiber-optic transponder with a host device ~~in order to control a logic level of a lock signal used by the host device~~, the method comprising:

receiving an asserted synchronization signal from a phase locked loop, the phase locked loop disposed on the controller chip;

determining whether the synchronization signal is caused by the phase locked loop locking onto a data signal or by the phase locked loop passing a hunting frequency through a data signal frequency; [[and]]

asserting a lock signal if the phase locked loop has locked onto a data signal;

sampling data from the data signal;

extracting a clock signal from the data signal; and

using the extracted clock signal as a reference for converting the sampled data into synchronized data to be read by the host device.

15. **(Original)** The method of claim 14, wherein determining whether the synchronization signal is caused by the phase locked loop locking onto a data signal or by the phase locked loop passing a hunting frequency through a data signal frequency further comprises:

measuring a period of time that the synchronization signal is asserted;

and

determining that the synchronization signal is caused by the phase locked loop locking onto the data signal if the period of time that the synchronization signal is asserted is greater than a specified period of time.

16. **(Original)** The method of claim 14, further comprising comparing the asserted synchronization signal with a reference signal to determine if the asserted synchronization signal is produced by the phase locked loop locking onto a data signal or by the phase locked loop passing a hunting frequency through the data signal frequency.

17. **(Previously Presented)** The method of claim 14, further comprising comparing the synchronization signal with a reference signal to produce the lock signal useful by a host device coupled to the fiber-optic transponder.

18. **(Original)** The method of claim 14, further comprising changing a logical level of the lock signal when the value of the lock signal changes by some value greater than a hysteresis threshold value.

19. **(Currently Amended)** In a system that generates a synchronization signal to indicate the presence of a data signal, a translation circuit comprising:

a timing circuit adapted to measure a period of time that the synchronization signal is asserted using at least a capacitor arranged to discharge when the synchronization signal is asserted and to charge when the synchronization signal is not asserted, wherein the timing circuit is further adapted to generate an output signal having a voltage across the capacitor; and

a comparator circuit adapted to compare the output signal with a reference signal such that a lock signal is not asserted unless the comparison of the output signal with the reference signal indicates that the period of time that the synchronization signal is asserted exceeds a minimum period of time.

20. **(Original)** The translation circuit of claim 19, wherein the timing circuit comprises a transistor that is controlled by the synchronization signal for resetting the timing circuit such that the capacitor discharges.

21. **(Original)** The translation circuit of claim 20, wherein the transistor is at least one of a PNP bipolar junction transistor, an NPN bipolar junction transistor, and a field effect transistor.

22. **(Original)** The translation circuit of claim 19, wherein the comparator circuit includes feedback that changes a logical level of the lock signal useful by the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value of the comparator circuit.

23. **(Original)** The translation circuit of claim 22, wherein the hysteresis threshold value of the comparator circuit prevents the lock signal from changing logic levels until the output signal of the timing circuit changes by an amount greater than the hysteresis threshold value.

24. **(Original)** The translation circuit of claim 22, further comprising an input level detector that passes the synchronization signal to the timing circuit when the synchronization signal exceeds a reference voltage.

25. **(Canceled)**

26. **(Currently Amended)** The translation circuit of claim 20 [[22]] wherein the capacitor is coupled to the transistor such that current flows through the transistor to charge the capacitor when the synchronization signal is asserted ~~adapted to charge~~ at a rate faster than a rate at which the capacitor discharges through a resistor coupled thereto, and wherein the comparator is adapted to assert the lock signal when the reference signal exceeds the voltage across the capacitor.

27. **(New)** The fiber-optic transponder of claim 9, wherein the data signal is an electronic data signal, the fiber-optic transponder further comprising circuitry to convert an optical data signal to the electronic data signal.

28. **(New)** The translation circuit of claim 19, wherein the capacitor is arranged such that a voltage across the capacitor is an average of the synchronization signal over a period of time.